



# IP Datasheet

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## Serial FPDP Gen3

for Xilinx, Altera, Microsemi, and Lattice FPGAs

Serial Front Panel Data Port Gen3 is a next-generation, high bandwidth serial communications protocol defined by the ANSI/VITA 17.3-2018 (R2025) standard. sFPDP-Gen3 supports single-lane or multi-lane links with automatic channel bonding and uses a 64B/67B framing layer to achieve over 95% bandwidth efficiency. sFPDP-Gen3 supports the same user data frame types found in the previous VITA 17.1 specification, allowing for easy system upgrades. The StreamDSP sFPDP Gen3 core now supports Forward Error Correction (FEC) with the StreamDSP StreamFEC IP core.

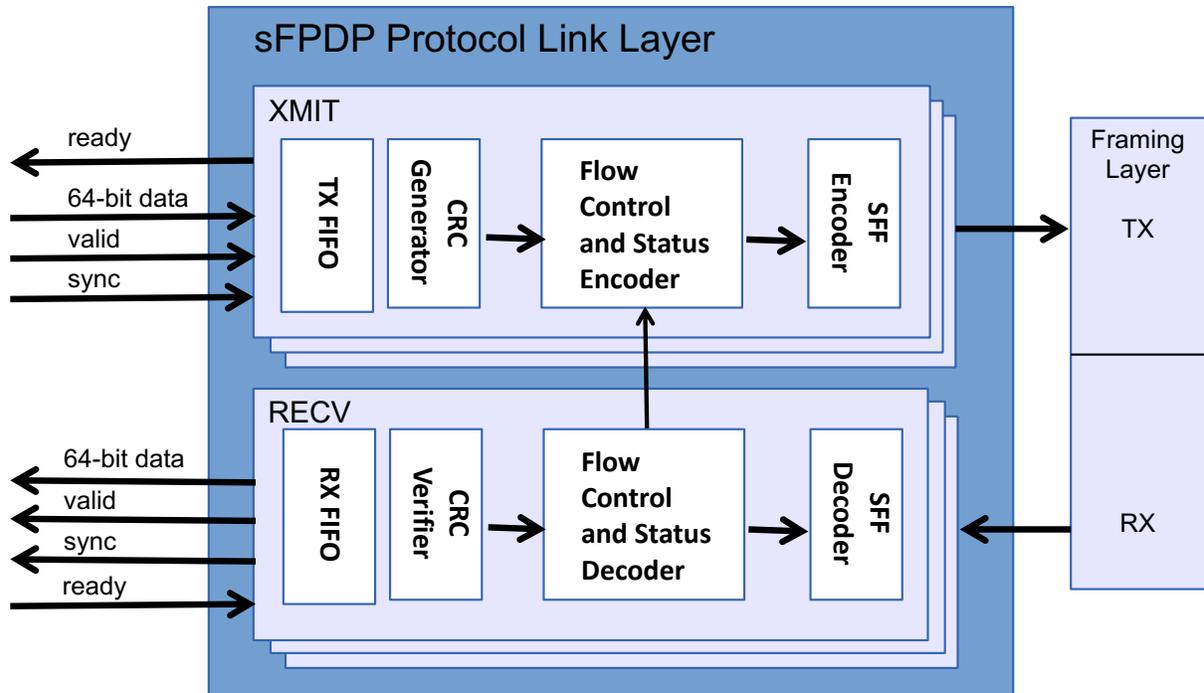
Serial FPDP Gen3 is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, and high-bandwidth video systems. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and supports flexible data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver-based devices from Xilinx, Altera, Microsemi, and Lattice. The core provides an open interface to the FPGA transceiver, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for each family, as well as a thorough testbench. In addition, we perform exhaustive interoperability testing among all FPGA families and manufacturers to ensure compatibility.

## Features

- ✓ Supports Forward Error Correction (FEC)
- ✓ VITA 17.3-2018 (R2025) Compliant
- ✓ Multi-lane channel bonding support
- ✓ 64B/67B Framing Layer
- ✓ Independent data / system clock domains
- ✓ Optional flow control and CRC24
- ✓ 64-bit user data interface
- ✓ Basic control/status interface
- ✓ Local and Far-End Link status
- ✓ Local UDB CRC24 validation
- ✓ Unidirectional and bidirectional support
- ✓ All sFPDP frame types supported
  - Unframed data
  - Single frame data
  - Fixed size repeating frame data
  - Dynamic size repeating frame data
- ✓ All sFPDP system configurations
  - Basic System
  - Flow Control
  - Bidirectional Data Flow

## Protocol Link Layer

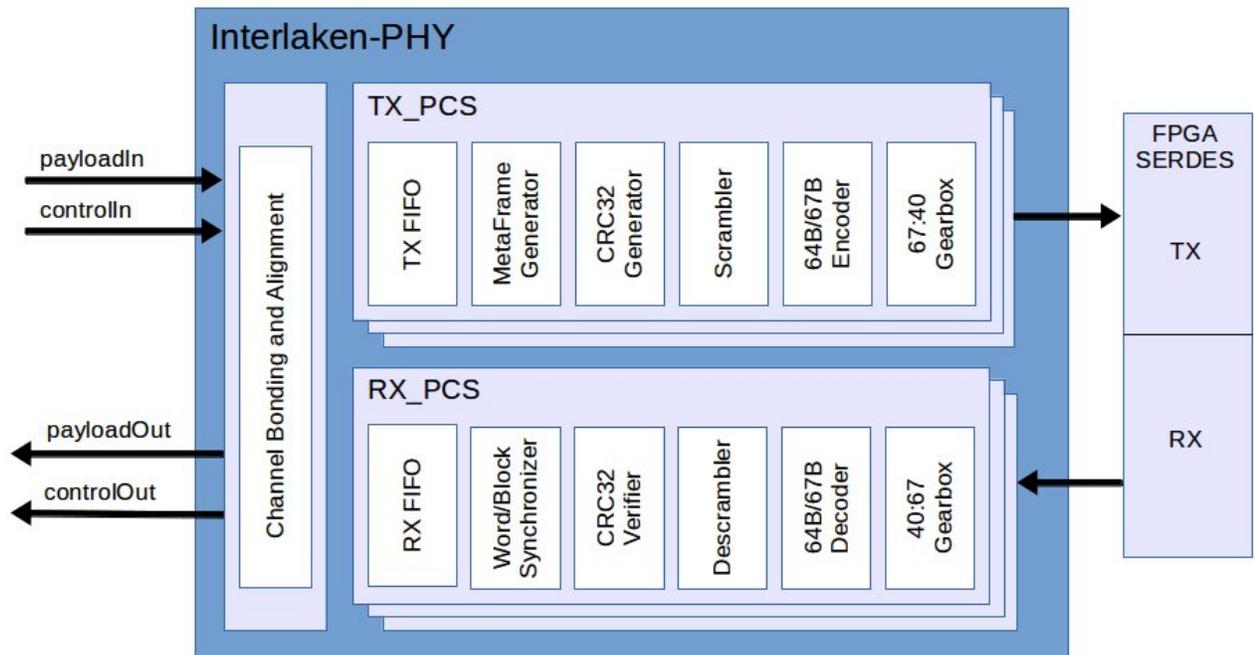


The sFPDP-Gen3 Protocol Link Layer accepts data from the user and implements the dual-clock domain transfer FIFOs and Serial Fiber Frame (SFF) encoding. The user data interface is 64-bits per lane, and the IP supports automatic flow control. User data is encoded/decoded into valid sFPDP Serial Fiber Frames (SFFs) based on the user's requested framing type and is sent to the Framing Layer for encapsulation into the Payload section of the Meta-Frame. Optional CRC24 is calculated to generate User Data Block (UDB) ACK\_GOOD and ACK\_BAD status flags to allow for guaranteed delivery mechanisms.

When Forward Error Correction (FEC) is enabled, the FEC Encoder and Decoder sit directly outside the transceiver to protect the integrity of the link.

# IP Framing Layer

## Datasheet



The sFPDP-Gen3 Framing Layer implements the 64B/67B Framing Layer defined by the Interlaken v1.3 specification. The Framing Layer supports single-lane and multi-lane channel bonding with automatic link synchronization. A per-lane CRC32 is calculated to guarantee link integrity and assist with channel diagnostics. The Framing Layer exchanges data between the sFPDP Protocol Link layer and the FPGA transceiver(s).

# IP

# Device Supp

## Datasheet

### FPGA Family Support

#### ALTERA

- Arria 5 GX
- Stratix 4 GX
- Stratix 5 GX
- Cyclone V
- Cyclone 10
- Arria 10 GX
- Stratix 10 GX
- Agilex

#### Example Design

Altera Arria-V GX Starter Development Kit  
Altera Stratix-IV GX PCIe Development Kit  
Altera Stratix-V GX PCIe Development Kit  
Intel Cyclone-V GX SoC FPGA Development Kit  
Intel Cyclone-10 FPGA Development Kit  
Intel Arria-10 GX FPGA Development Kit  
Intel Stratix-10 GX FPGA Development Kit (L-Tile, H-Tile, E-Tile)  
Intel Agilex I-Series and F-Series FPGA Development Kit

#### XILINX

- Virtex-6 LXT
- Virtex-7 GTH
- Virtex-7 GTX
- Artix UltraScale+
- Artix-7 GTP
- Kintex-7 GTX
- Kintex UltraScale
- Virtex UltraScale
- Virtex Ultracale+
- Kintex UltraScale+
- Zynq UltraScale+ MPSoC
- Zynq UltraScale+ RFSoc
- Versal ACAP
- Alveo

Xilinx ML605 Development Kit  
Xilinx VC709 Evaluation Kit  
Xilinx VC707 Evaluation Kit  
phantom board  
Xilinx AC701 Development Kit  
Xilinx KC705 Development Kit  
Xilinx KCU105 Development Kit  
Xilinx VCU108 Development Kit  
Xilinx VCU118 Development Kit  
Xilinx KCU116 /development Kit  
Xilinx ZCU102 MPSoC Development Kit  
Xilinx ZCU111 RFSoc Development Kit  
Xilinx VCK190 Evaluation Board  
Xilinx Alveo U200 Data Center Accelerator Card

#### MICROSEMI

- PolarFire

Arrow Everest PolarFire Development Kit

#### LATTICE

- Avant G/X

Lattice Avant G/X Versa Development Kit

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).

\*\*\* Additional FPGA families are actively being worked on. Our goal is to support ALL transceiver-based FPGA families. If you need support for an FPGA family not listed above, please let us know ASAP and we can help prioritize our rollout schedule for you!

