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IP Datasheet

Serial FPDP Gen3

for Altera, Xilinx, and Microsemi FPGAs

Serial Front Panel Data Port Gen3 is a next-generation, high bandwidth serial communications protocol defined by the ANSI/VITA 17.3-2018 standard. sFPDP-Gen3 supports single-lane or multi-lane links with automatic channel bonding and uses a 64B/67B framing layer to achieve over 95% bandwidth efficiency. sFPDP-Gen3 supports the same user data frame types found in the previous VITA 17.1 specification, allowing for easy system upgrades. Serial FPDP Gen3 is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, signal processing, data recording, and high-bandwidth video systems. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and easily supports different types of data with efficient and flexible data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver-based devices from Intel/Altera, Xilinx, and Microsemi. We're always making improvements to the core and adding support for new FPGA device families. Our core provides an open interface to the FPGA transceiver, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for each family, as well as a thorough testbench with support for Riviera and ModelSim tools. In addition, our testing procedure includes exhaustive interoperability testing among all FPGA families and manufacturers to ensure compatibility.

StreamDSP is committed to delivering the highest level of customer support to ensure smooth system integrations. We also offer IP core customization and FPGA design services.

Features

- ☑ VITA 17.3-2018 Compliant
- ☑ Multi-lane channel bonding support
- ☑ 64B/67B Framing Layer
- ☑ Independent data / system clock domains
- ☑ Optional flow control and CRC24
- ☑ 64-bit user data interface
- ☑ Basic control/status interface
- ☑ Local and Far-End Link status
- ☑ Local UDB CRC24 validation
- ☑ Unidirectional and bidirectional support
- ☑ All sFPDP frame types supported
  - Unframed data
  - Single frame data
  - Fixed size repeating frame data
  - Dynamic size repeating frame data
- ☑ All sFPDP system configurations
  - Basic System
  - Flow Control
  - Bidirectional Data Flow

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Protocol Link Layer

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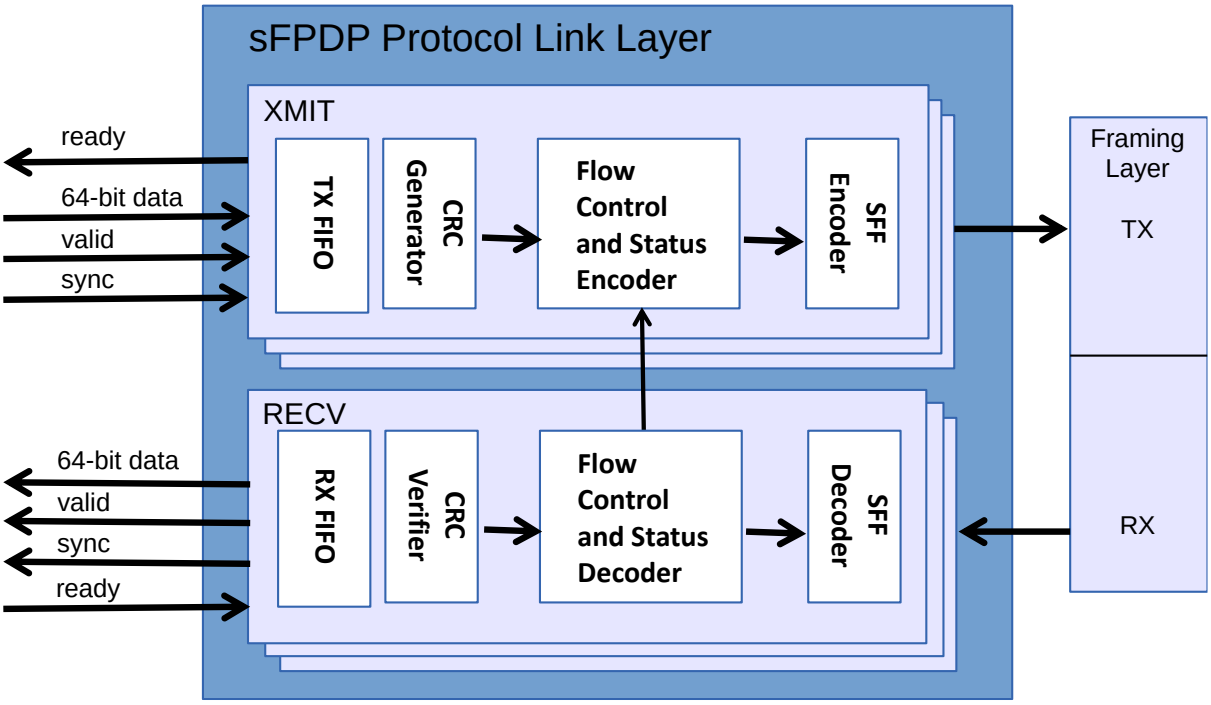

The sFPDP-Gen3 Protocol Link Layer accepts data from the user and implements the dual-clock domain transfer FIFOs and Serial Fiber Frame (SFF) encoding. The user data interface is 64-bits per lane, and the IP supports automatic flow control. User data is encoded/decoded into valid sFPDP Serial Fiber Frames (SFFs) based on the user's requested framing type and is sent to the Framing Layer for encapsulation into the Payload section of the Meta-Frame. Optional CRC24 is calculated to generate User Data Block (UDB) ACK_GOOD and ACK_BAD status flags to allow for guaranteed delivery mechanisms.

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Framing Layer

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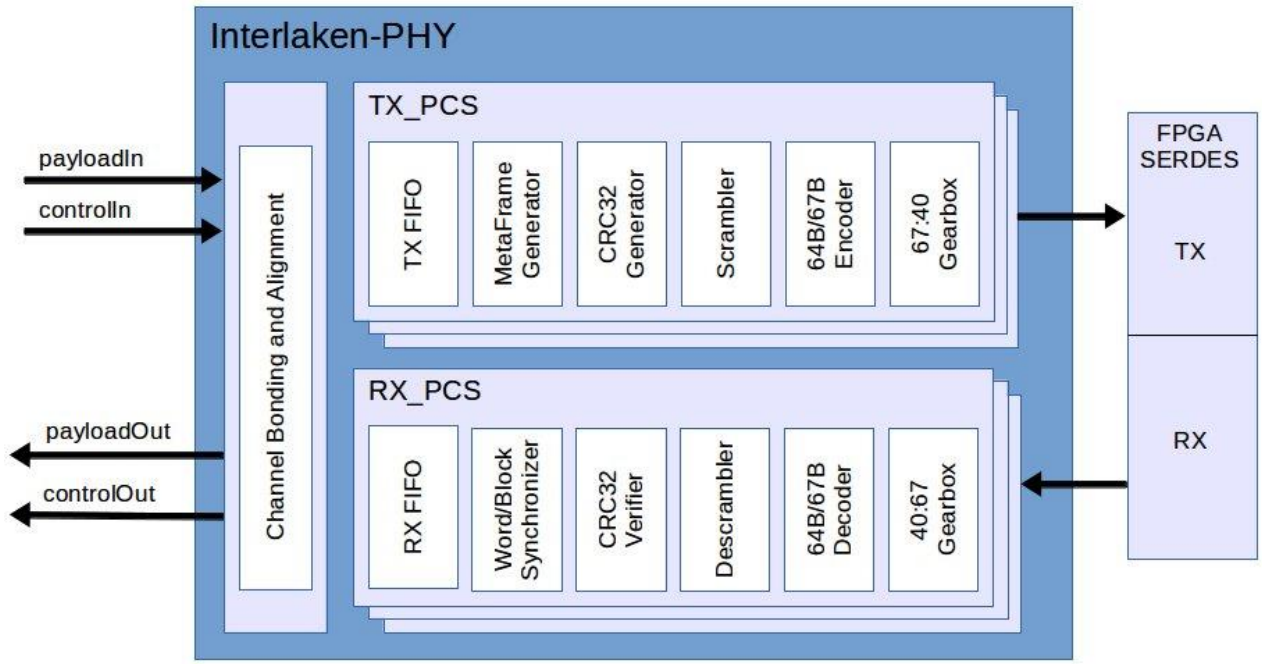

The sFPDP-Gen3 Framing Layer implements the 64B/67B Framing Layer defined by the Interlaken v1.3 specification. The Framing Layer supports single-lane and multi-lane channel bonding with automatic link synchronization. A per-lane CRC32 is calculated in order to guarantee link integrity and assist with channel diagnostics. The Framing Layer exchanges data between the sFPDP Protocol Link layer and the FPGA transceiver(s).

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Device Support

FPGA Family Support

ALTERA	Example Design
• Arria 5 GX	Altera Arria-V GX Starter Development Kit
• Stratix 4 GX	Altera Stratix-IV GX PCIe Development Kit
• Stratix 5 GX	Altera Stratix-V GX PCIe Develoment Kit
• Arria 10 GX	Altera Arria-10 GX FPGA Development Kit
• Stratix 10 GX	Altera Stratix-10 GX FPGA Development Kit (L-Tile and H-Tile)
XILINX	
• Virtex-6 LXT	Xilinx ML605 Development Kit
• Virtex-7 GTH	Xilinx VC709 Evaluation Kit
• Virtex-7 GTX	Xilinx VC707 Evaluation Kit
• Artix-7 GTP	Xilinx AC701 Development Kit
• Kintex-7 GTX	Xilinx KC705 Development Kit
• Kintex UltraScale GTH	Xilinx KCU105 Development Kit
• Virtex UltraScale GTH/GTY	Xilinx VCU108 Development Kit
• Virtex Ultracale+ GTY	Xilinx VCU118 Development Kit
• Zynq UltraScale+ GTH	Xilinx ZCU102 MPSoC Development Kit

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).

*** Additional FPGA families are actively being worked on. Our goal is to support ALL transceiver-based FPGA families. If you need support for an FPGA family not listed above, please let us know ASAP an we can help prioritize our rollout schedule for you!